Amendments to the Specification:

Please add the following new paragraph immediately following the title on page 1:

--CROSS-REFERENCE TO RELATED APPLICATION(S)

This application is a divisional of U.S. Serial No. 09/652,044, filed August 31, 2000.--

Please replace the paragraph beginning at page 8, line 21, with the following amended paragraph:

-- A method of manufacturing various MOS transistors composing the driver for driving a liquid crystal will be described below. The semiconductor of the present invention is applicable to various drivers such as a liquid crystal driver.--

Please replace the paragraph beginning at page 9, line 22 to page 10, line 15, with the following amended paragraph:

--Next, a first low concentration N-type ~~source~~ and P-type source/drain layers (hereinafter called an LN layer 10 and an LP layer 11) are formed using a resist film as a mask. That is, first, phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of $8 \times 10^{12}/cm^2$ in a state that an area except an area where the LN layer is formed is covered with a resist film not shown so as to form the LN layer 10. Afterward, boron ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of $8.5 \times 10^{12}/cm^2$ in a state that an area except an area where the LP layer is formed is covered with a resist film (PR) so as to form the LP layer 11. Actually, each ion implanted as described above is thermically diffused after an annealing process (for example, for two hours in the atmosphere of N_2 of 1100°C) which is a postprocess to be the LN layer 10 and the LP layer 11.--

Please replace the paragraph beginning at page 10, line 16 to page 11, line 13, with the following amended paragraph:

--Next, as shown in Figs. 3, a second-low concentration N-type source drain layers (hereinafter called an SLN layer 13 ~~SLP layer 14~~) are formed between the LN layers 10 using a resist film as a mask and a ~~surface~~ second-low concentration P-type source drain layers (hereinafter called an SLP layer 14) is formed between the LP layers 11 using a resist film as a mask. That is, first phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of $1.5 \times 10^{12}/cm^2$ in a state that an area except an area where the SLN layer is formed is covered with a resist film not shown so as to form the SLN layer 13 which ranges to the LN layer 10. Afterward, boron difluoride ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 140 KeV under the implantation condition of $2.5 \times 10^{12}/cm^2$ in a state that an area except an area where the SLP layer is formed is covered with a resist film (PR) so as to form the SLP layer 14 which ranges to the LP layer 11. The impurity concentration of to the LN layer 10 and the SLN layer 13, or the LP layer 11 and the SLP layer 14 are set respectively substantially equal or one of them is higher then others.--

Please replace the paragraph beginning at page 11, line 14 to page 12, line 4, with the following amended paragraph:

--Further, as shown in Figs. 4, high concentration N-type ~~source~~ and P-type source/drain layers (hereinafter called an N+ layer 15 and a P+ layer 16) are formed using a resist layer as a mask. That is, first, phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 80 KeV under the implantation condition of $2 \times 10^{15}/cm^2$ in a state that an area except an area where the N+ layer is formed is covered with a resist film not shown so as to form the N+ layer 15 which ranges to the LN layer 10. Afterward, boron difluoride ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 140 KeV under the implantation condition of $2 \times 10^{15}/cm^2$ in a state that an area except an area where the P+ layer is formed is covered with a resist film (PR) so as to form the P+ layer 16.--

Please replace the paragraph beginning at page 13, line 7 to page 14, line 6, with the following amended paragraph:

--That is, boron ions are similarly implanted into the superficial layer of the substrate at the acceleration voltage of approximately 50 KeV under a second implantation condition of 2.6 x $10^{15}/cm^2$ in a state that an area except an area where the P-type layer is formed is covered with a resist film not shown so as to form the second P-type well 21 after boron ions for example are implanted into the P-type well 3 at the acceleration voltage of approximately 190 KeV under a first implantation condition of 1.5 x $10^{13}/cm^2$ using a resist film not shown having its opening on an area where the N-channel MOS transistor is formed for normal resistance to voltage as a mask. Also, phosphorus ions for example are implanted into the P-type well 3 at the acceleration voltage of approximately 380 KeV under the implantation condition of 1.5 x $10^{13}/cm^2$ using a resist film (PR) having its opening on an area where the P-channel MOS transistor is formed for normal resistance to voltage as a mask so as to form the second N-type well 22. In case a generator of the acceleration voltage of approximately 380 KeV is not provided, ~~a double charging method in which phosphorus ion is implanted at the acceleration voltage of 190 KeV under the implantation condition of 1.5 x $10^{13}/cm^2$ and then phosphorus ion is implanted at the acceleration voltage of 150 KeV under the implantation condition of 4.0 $10^{12}/cm^2$ may be also adopted~~. A double charging method in which bivalent phosphorus ion is implanted at the acceleration voltage of 190 keV under the implantation condition of 1.5 x $10^{13}/cm^2$ may be also adopted. Subsequently phosphorus ion is implanted at the acceleration voltage of 150 keV under the implantation condition of 4.0 x $10^{12}/cm^2$.